

UNITED STATES PATENT APPLICATION

for

A Method and Apparatus for Self-Aligned MOS Patterning

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## BACKGROUND OF THE INVENTION

### 1. FIELD OF THE INVENTION

[0001] The present invention relates to the field of semiconductor device fabrication, and in particular to lithography patterning of thin film stacks for lithography using light having a wavelength of 193nm or less.

### 2. DISCUSSION OF RELATED ART

[0002] Present semiconductor fabrication techniques may be used to generate single electrode transistor gates using 193nm wavelength lithography technology or dual electrode flash memory transistor gates using 248nm wavelength lithography technology.

[0003] Figure 1 illustrates a flash memory transistor gate stack. The flash memory gate stack is formed on substrate 100. The gate stack of the flash memory transistor consists of a control gate electrode layer 108 deposited over an inter-electrode dielectric 106, over a floating gate layer 104, over the gate dielectric 102, on a substrate 100. Source/drain spacer liner dielectric 140 is formed on either side of the flash memory gate stack. Source/drain spacer dielectric 142 is formed on either side of the gate stack on top of the source/drain spacer liner dielectric 140.

[0004] Figure 2 illustrates the flash memory gate stack after the resist has been patterned using light 280 having a wavelength of 248nm or greater. The thickness of the resist 214 is bounded by etch resistance and patterning resolution. The flash transistor gate is etched using a Self-Aligned MOS (SAMOS) process. The SAMOS process allows all layers of the flash transistor gate stack to be etched using the resist as a mask, including the gate dielectric 202, the floating gate electrode 204, the interelectrode dielectric 206, and the control gate electrode 208.

[0005] To achieve high resolution patterning with 193nm (or less) lithography for flash transistors, a change in resist formulation is required. The resist formulation for 193nm lithography compromises the ability of the resist to withstand the environment required to etch the SAMOS flash gate stack, and is not stable in etch chemistries. Thus, it is undesirable to use resist as a mask to etch the flash SAMOS gate stack using 193nm or less lithography.

[0006] Hardmask materials that consist of similar elements to those found in the inter-poly dielectric layer, such as a nitride layer, are also undesirable for use as a SAMOS mask. These materials may be compromised during the etch process. Furthermore, the removal of a hardmask consisting of a similar material as the inter-poly dielectric layer may compromise the dielectric and lead to device failure.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0007] **Figure 1** is an illustration of a cross-sectional view of a flash memory transistor.

[0008] **Figure 2** is an illustration of a cross-sectional view of the flash memory transistor gate stack with patterned resist.

[0009] **Figure 3** is a flow diagram illustrating a process in accordance with one embodiment of the present invention.

[0010] **Figure 4** is an illustration of a cross-sectional view of an initial thin film stack in accordance with one embodiment of the present invention.

[0011] **Figure 5** is an illustration of a cross-sectional view of the thin film stack after the ARC has been patterned using lithography in accordance with one embodiment of the present invention.

[0012] **Figure 6** is an illustration of a cross-sectional view of the thin film stack after the hardmask has been etched in accordance with one embodiment of the present invention.

[0013] **Figure 7** is an illustration of a cross-sectional view of the thin film stack after the control gate has been etched in accordance with one embodiment of the present invention.

[0014] **Figure 8** is an illustration of a cross-sectional view of the thin film stack after the interelectrode dielectric has been etched in accordance with one embodiment of the present invention.

[0015] **Figure 9** is an illustration of a cross-sectional view of the thin film stack after the entire thin film stack has been etched in accordance with one embodiment of the present invention.

[0016] **Figure 10** is an illustration of a cross-sectional view of the thin film stack after the removal of the hardmask in accordance with one embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0017] In the following description, numerous specific details are set forth, such as exact process steps, in order to provide a through understanding of the present invention. It will be apparent, however, that these specific details need not be employed to practice the present invention. In other instances, well known components or methods have not been described in detail in order to avoid unnecessarily obscuring the present invention.

[0018] Figure 3 is a flow diagram 300 which illustrates a process in accordance with one embodiment of the present invention. Flow diagram 300 illustrates a general method of patterning and etching a thin film stack using a hardmask layer.

[0019] First, as shown in block 302, a thin film stack is formed. The thin film stack may include at least a poly silicon layer and an oxide layer on a substrate. In one embodiment, the thin film stack may be a flash memory gate stack. For simplicity, the thin film stack describe herein and illustrated in Figures 1, 2, and 4-10 is a flash memory gate stack, however, any thin film stack containing at least a polysilicon layer and an oxide layer may be substituted in other embodiments of the present invention.

[0020] Figure 4 illustrates an exemplary flash memory gate stack 420. A gate dielectric layer 402 is grown or deposited on substrate 400. Substrate 400 may be a silicon substrate. The substrate may be comprised of a material other than silicon, including, but not limited to, materials such as gallium arsenide, or silicon on insulator (SOI) substrates. In one embodiment, the gate dielectric may comprise a silicon oxide or silicon oxynitride. After the gate oxide layer 402 is formed, the floating gate electrode layer 404 is deposited. The floating gate layer 404 may comprise an n-type polysilicon layer. Next, the interelectrode dielectric 406 is formed. The interelectrode dielectric 406 may comprise an ONO (oxide-nitride-oxide) layer. Finally, the control gate electrode layer 408 is formed. The control gate electrode 408 may comprise polysilicon.

[0021] Next, as illustrated in Figure 3, block 304, a hardmask layer is formed over the thin film stack. The hardmask layer is illustrated in Figure 4. Figure 4 shows the hardmask

layer 410 formed over the top surface of thin film stack 420, which in one embodiment may be a flash memory gate stack. The hardmask material must be resistant to both common polysilicon etch chemistries as well as oxide etch chemistries. The hardmask material must also have optical properties with a favorable extinction coefficient for 193nm wavelength light. For future lithography nodes, the hardmask material must have optical properties that are favorable for light having wavelengths of less than 193nm. In one embodiment, the hardmask layer may be a carbon-based layer, and may comprise a pure amorphous carbon layer. Applied Materials® Advanced Patterning Film™ (APF™) may be used for the hardmask. The hardmask layer may be formed to a thickness of 1000 to 3000Å.

[0022] After the hardmask layer is formed, an anti-reflective coating (ARC) layer is formed over the hardmask layer, as illustrated in Figure 3, block 306.

[0023] Figure 4 illustrates the ARC layer 412 formed over the top surface of the hardmask layer. The ARC layer may be comprised of silicon dioxide, silicon oxynitride or a composite thereof. The ARC layer reduces undesirable light reflections by phase shift cancellation, which is dependent upon the extinction coefficient and the thickness of the film. The ARC material must have optical properties with a favorable extinction coefficient for 193nm lithography. For future lithography nodes, the ARC material must have optical properties that are favorable for light having wavelengths of less than 193nm. The ARC layer may be formed to a thickness of 100 to 500Å.

[0024] Using photoresist, the ARC layer is then patterned to define the flash gate, as illustrated in Figure 3, block 308. The photoresist may be patterned using standard 193nm wavelength light, 480, as shown in Figure 5. Lithography using light having a wavelength of less than 193nm may also be used.

[0025] Figure 5 illustrates the thin film stack after the ARC layer 412 has been patterned with photoresist 414. The resist formulation must be appropriate for 193nm lithography. Resist 414 may be formed to a thickness of 2000 to 5000Å. The resist thickness may be optimized for patterning resolution only, and does not require etch resistance consideration. Standard etch chemistries may be used to define the pattern in the ARC.

Since the etch chemistry used typically will have a high selectivity to photoresist, this is also the pattern transfer step for the lithography. Because both the resist 414 and the hardmask 410 may be comprised of carbon, the ARC layer 412 prevents the hardmask 410 from being breached during the etch process.

[0026] After the ARC layer has been patterned, the hardmask layer and the thin film stack may be etched, as set forth in Figure 3, block 310.

[0027] Figure 6 illustrates the hardmask etch. The patterned ARC layer 412 is used as a mask to etch the hardmask layer 410. A standard etch chemistry may be used to etch the hardmask. In one embodiment, the hardmask may be etched using an oxygen and argon etch chemistry. Much of the resist 414 may be removed by the hardmask etch process. This is because both the hardmask and the resist are composed of carbon based materials. An etch chemistry which etches the hardmask will also etch the resist.

[0028] After the pattern has been transferred from the ARC layer 412 to the hardmask layer 410, the hardmask layer may be used as a mask to etch the remainder of the thin film stack because the hardmask material is selective to both the polysilicon and oxide etch chemistries.

[0029] Figure 7 illustrates the control gate etch. Hardmask 410 is used as a mask to pattern the control gate 408. The hardmask is selective to the polysilicon etch chemistry, and remains intact after the control gate is etched.

[0030] The ARC layer needs to remain intact only for the duration of the hardmask etch, since the hardmask has a high selectivity to both the polysilicon and oxide etch chemistries. The ARC layer 412 may be completely removed by the first polysilicon etch process.

[0031] Figure 8 illustrates the interelectrode dielectric etch. Hardmask 410 is used as a mask to pattern the interelectrode dielectric 406. The hardmask is selective to the dielectric etch chemistry, and remains intact after the interelectrode dielectric is etched. If any portion of the ARC layer remains on the top surface of the hardmask 410 after the first polysilicon etch process, it will be completely removed during the interelectrode dielectric

etch. This is because the ARC layer and the interelectrode dielectric typically have similar physical properties and may be composed of similar materials.

[0032] Figure 9 illustrates the thin film stack after all layers have been etched, including the control gate 408, interelectrode dielectric 406, floating gate 404, and gate dielectric 402. The hardmask 410 is used as a mask for etching each of the layers. All layers may be etched during a single manufacturing step in the same chamber, however different etch chemistries may be required to etch different layers. The hardmask used to pattern each of the layers remains intact after the etch process is complete.

[0033] After the thin film stack has been etched, the hardmask layer may be removed. A conventional cleaning process, such as a standard resist removal process, may be used to volatilize the hardmask material and prepare the surface for further processing. In one embodiment, the hardmask may be removed using an oxygen plasma ash. Figure 10 illustrates the thin film stack 420 after all layers have been etched and after the hardmask layer has been removed. The remaining etched thin film layers may comprise a flash memory gate stack, including control gate 408, interelectrode dielectric 406, floating gate 404, and gate dielectric 402.

[0034] The present invention may be implemented with various changes and substitutions to the illustrated embodiments. For example, the present invention may be implemented on various types of thin film stacks having different heights and comprising different materials. The present invention is not limited only to flash memory gate stacks. Furthermore, the present invention may be implemented on flash memory gates whose gate stacks vary from those described herein. For example, a flash memory gate stack may contain additional or different layers than those described herein.

[0035] Although specific embodiments, including specific parameters, methods, and materials have been described, it will be readily understood by those skilled in the art and having the benefit of this disclosure, that various other changes in the details, materials, and arrangements of the materials and steps which have been described and illustrated in



order to explain the nature of this invention may be made without departing from the principles and scope of this invention as expressed in the subjoined claims.